CLAIMS

1. A field emission display baseplate comprising:

a substrate;

a plurality of spaced-apart conductors formed on the substrate;

a plurality of spaced-apart emitter bodies comprising a high resistivity material formed on the conductors;

a dielectric layer formed on the substrate and the conductors, the silicon dioxide layer having respective openings coaxial with the emitter bodies;

an extraction grid formed on the porous silicon dioxide layer and including respective openings coaxial with the emitter bodies;

; and

an emitter tip formed on each of the emitter bodies in the extraction grid opening, the tip formed from a material having a work function or electron affinity of less than four electron volts.

2. The baseplate of claim 1 wherein the dielectric layer comprises porous silicon dioxide prepared by anodization of polycrystalline silicon followed by oxidation of the anodized polycrystalline silicon.

3. The baseplate of claim 1 wherein the dielectric layer comprises at least 50% voids.

4. The baseplate of claim 1 wherein the dielectric layer has a relative dielectric constant of less than three.

5. The baseplate of claim 1 wherein the porous dielectric layer has a relative dielectric constant of less than 1.6.

6. The baseplate of claim 1 the dielectric layer comprises porous silicon dioxide prepared by chemical etching of polycrystalline silicon followed by oxidation of the etched polycrystalline silicon.

7. The baseplate of claim 1 wherein the emitter tip comprises a material chosen from a group consisting of: SiC, Zr, La, Zn, TiN, LaB_6, Ce, Ba, diamond and silicon oxycarbide.

8. The baseplate of claim 1 wherein the emitter body comprises:

silicon monoxide; and

a metal.

9. The baseplate of claim 1 wherein the emitter body comprises:

silicon monoxide; and

less than 10 atomic percent manganese.

10. A field emission display baseplate comprising:

a substrate;

a plurality of conductors formed on the substrate;

a plurality of emitters each formed on one of the plurality of conductors;

a porous silicon dioxide layer formed by anodization on the substrate and the conductors;

an extraction grid formed on the dielectric layer and including an opening;

an opening formed in the dielectric layer coaxial with the opening in the extraction grid;

an emitter body comprising a high resistivity material formed in the opening in the porous silicon dioxide layer; and

an emitter tip formed on the emitter body and in the extraction grid opening, the tip formed from a material having a work function or electron affinity of less than four electron volts.

11. The baseplate of claim 10 wherein the porous silicon dioxide comprises porous silicon dioxide prepared by anodization of polycrystalline silicon followed by oxidation of the anodized polycrystalline silicon.

12. The baseplate of claim 10 wherein the porous silicon dioxide comprises at least 50% voids.

13. The baseplate of claim 10 wherein the porous silicon dioxide has a relative dielectric constant of less than three.

14. The baseplate of claim 10 wherein the porous silicon dioxide has a relative dielectric constant of less than 1.6.

15. The baseplate of claim 10 the porous silicon dioxide comprises porous silicon dioxide prepared by chemical etching of polycrystalline silicon followed by oxidation of the etched polycrystalline silicon.

16. A field emission display baseplate comprising:

a substrate;

a plurality of spaced-apart conductors formed on the substrate;

a porous silicon dioxide layer formed on the substrate and the conductors by a modification of a silicon layer;

an extraction grid formed on the porous silicon dioxide layer and including an opening;

an opening formed in the porous silicon dioxide layer coaxial with the opening in the extraction grid; and

an emitter formed in the opening in the porous silicon dioxide layer and in the extraction grid opening.

17. The baseplate of claim 16 wherein the porous silicon dioxide layer comprises silicon dioxide prepared by anodization of polycrystalline silicon followed by oxidation of the anodized polycrystalline silicon.

18. The baseplate of claim 16 wherein the porous silicon dioxide comprises at least 50% voids.

19. The baseplate of claim 16 wherein the porous silicon dioxide has a relative dielectric constant of less than three.

20. The baseplate of claim 16 wherein the porous silicon dioxide has a relative dielectric constant of less than 1.6.

21. The baseplate of claim 16 wherein the porous silicon dioxide comprises silicon dioxide prepared by chemical etching of silicon to provide porous silicon followed by oxidation of the porous silicon.

22. The baseplate of claim 16 wherein emitter comprises:

an emitter body comprising a high resistivity material; and

an emitter tip formed on the emitter body and in the extraction grid opening.

23. The baseplate of claim 22 wherein the emitter tip comprises a material chosen from a group consisting of: SiC, Zr, La, Zn, TiN, LaB_6, Ce, Ba, diamond and silicon oxycarbide.

24. The baseplate of claim 22 wherein the emitter body comprises:

silicon monoxide; and

a metal.

25. The baseplate of claim 22 wherein the emitter body comprises:

silicon monoxide; and

less than 10 atomic percent manganese.

26. A field emission display comprising:

a substrate;

a plurality of emitters formed on the substrate, each of the emitters being formed on a conductor;

a porous dielectric layer formed on the substrate, the porous dielectric layer having an opening formed about each of the emitters, the porous dielectric layer having a thickness substantially equal to a height of the emitters above the substrate, the porous layer formed by oxidation of porous silicon;

an extraction grid extraction grid formed substantially in a plane defined by respective tips of the plurality of emitters and having an opening surrounding each tip of a respective one of the emitters; and

a cathodoluminescent-coated faceplate having a planar surface formed parallel to and near the plane of tips of the plurality of emitters.

27. The display of claim 26 wherein the porous silicon dioxide comprises at least 50% voids.

28. The display of claim 26 wherein the porous silicon dioxide has a relative dielectric constant of less than three.

29. The display of claim 26 wherein the porous silicon dioxide has a relative dielectric constant of less than 1.6.

30. The display of claim 26 wherein the porous silicon is formed by anodization of a polycrystalline silicon layer.

31. The display of claim 26 wherein each of the emitters comprise:

an emitter body comprising a high resistivity material; and

an emitter tip formed on the emitter body and in the extraction grid opening.

32. The display of claim 31 wherein:

the emitter tips each comprise a material chosen from a group consisting of: SiC, Zr, La, Zn, TiN, LaB_6, Ce, Ba, diamond and silicon oxycarbide; and

the emitter bodies each comprise a cermet material.

33. The baseplate of claim 31 wherein the emitter bodies each comprise:

silicon monoxide; and

less than 10 atomic percent metal.

34. A computer system comprising:

a central processing unit;

a memory device coupled to the central processing unit, the memory device storing instructions and data for use by the central processing unit;

an input interface; and

a display, the display comprising:

a cathodoluminescent layer formed on a conductive surface of a transparent faceplate;

a substrate disposed parallel to and near the cathodoluminescent layer formed on the faceplate;

a plurality of conductors formed on the substrate;

a plurality of emitters formed on the conductors;

a porous silicon dioxide layer formed on the substrate and the columns, the porous silicon dioxide layer including openings each formed about one of the emitters, the porous layer formed by oxidation of porous silicon; and

an extraction grid formed on the porous silicon dioxide layer and including openings each coaxial with one of the openings in the porous silicon dioxide layer.

35. The computer system of claim 34 wherein the porous silicon dioxide has a relative dielectric constant of less than three.

36. The computer system of claim 34 wherein the porous silicon dioxide has a relative dielectric constant of less than 1.6.

37. The computer system of claim 34 wherein the porous silicon is formed by anodization of a polycrystalline silicon layer.

38. The computer system of claim 34 wherein each of the emitters comprises:

an emitter body comprising a high resistivity material; and

an emitter tip formed on the emitter body and in the extraction grid opening.

39. The computer system of claim 38 wherein:

the emitter tips each comprise a material chosen from a group consisting of: SiC, Zr, La, Zn, TiN, LaB_6, Ce, Ba, diamond and silicon oxycarbide; and

the emitter bodies each comprise a cermet material.

40. The computer system of claim 38 wherein the emitter bodies each comprise:

silicon monoxide; and

less than 10 atomic percent metal.

41. The computer system of claim 38 wherein tips of the emitters are formed from materials having a work function of less than four electron volts.

42. A method of fabricating a field emission display baseplate comprising:

forming columns on a substrate;

forming a layer of silicon on the columns and the substrate;

etching the silicon layer to form a layer of porous silicon;

oxidizing the porous silicon layer to form a layer of porous silicon dioxide;

forming an extraction grid on the porous silicon dioxide layer;

etching openings through the porous silicon dioxide and the extraction grid; and

forming emitters in the openings in the porous silicon dioxide and the extraction grid.

43. The method of claim 42 wherein the act of oxidizing the porous silicon layer to form a layer of porous silicon dioxide comprises oxidizing the porous silicon layer to form a layer of porous silicon dioxide having a relative dielectric constant of less than three.

44. The method of claim 42 wherein the act of oxidizing the porous silicon layer to form a layer of porous silicon dioxide comprises oxidizing the porous silicon layer to form a layer of porous silicon dioxide having a relative dielectric constant of less than 1.6.

45. The method of claim 42 wherein the act of oxidizing the porous silicon layer to form a layer of porous silicon dioxide comprises oxidizing a porous polycrystalline silicon layer to form a layer of porous silicon dioxide having an interior volume that is at least 50% voids.

46. The method of claim 42 wherein the act of etching the silicon layer to form a layer of porous polycrystalline silicon comprises anodizing a polycrystalline silicon layer to form a layer of porous polycrystalline silicon.

47. The method of claim 42 wherein the act of forming emitters comprises forming a high resistance emitter body of silicon monoxide and metal.

48. The method of claim 47 wherein the act of forming a high resistance emitter body comprises forming a high resistance emitter body by co-evaporation of silicon monoxide and a metal at an evaporation angle of 90 degrees with respect to the substrate surface.

49. The method of claim 42, further comprising, after the act of etching openings through the porous silicon dioxide and the extraction grid and prior to the act of forming emitters in the openings in the porous silicon dioxide and the extraction grid, forming a sacrificial layer on the extraction grid by angle evaporation.

50. The method of claim 49 wherein the act of forming a sacrificial layer on the extraction grid by angle evaporation comprises forming a sacrificial layer on the extraction grid by angle evaporation at an angle of seventy five degrees or more from a surface normal of the substrate.

51. The method of claim 49 wherein the act of forming emitters comprises:

forming emitter bodies by co-evaporating silicon monoxide and a metal; and

forming emitter tips by evaporating a material having a work function of less than four electron volts.

52. A method of fabricating a porous dielectric layer in a field emission display comprising:

forming a polycrystalline silicon layer on a substrate and a plurality of columns on the substrate;

forming pores in the polycrystalline silicon layer; and

oxidizing the polycrystalline silicon layer to provide a porous silicon dioxide layer.

53. The method of claim 52 wherein the act of forming pores in the polycrystalline silicon layer comprises anodizing the polycrystalline silicon layer.

54. The method of claim 52 wherein the act of oxidizing the polycrystalline silicon layer comprises thermally oxidizing the polycrystalline silicon layer at a temperature in excess of 950°C.

55. The method of claim 52 wherein the act of oxidizing the polycrystalline silicon layer comprises plasma oxidizing the polycrystalline silicon layer at a temperature in excess of 450°C.

56. A method of fabricating a field emission display baseplate comprising:

forming conductors on a substrate;

forming a layer of silicon dioxide on the conductors and on the substrate;

forming an extraction grid on the porous silicon dioxide layer;

etching openings through the silicon dioxide and the extraction grid; and

forming emitters in the openings in the porous silicon dioxide and the extraction grid.

57. The method of claim 56 wherein the act of forming emitters comprises forming a high resistance emitter body of silicon monoxide and metal.

58. The method of claim 57 wherein the act of forming a high resistance emitter body comprises forming a high resistance emitter body by

co-evaporation of silicon monoxide and a metal at an evaporation angle of 90 degrees with respect to the substrate surface.

59. The method of claim 56, further comprising, after the act of etching openings through the porous silicon dioxide and the extraction grid and prior to the act of forming emitters in the openings in the porous silicon dioxide and the extraction grid, forming a sacrificial layer on the extraction grid by angle evaporation.

60. The method of claim 59 wherein the act of forming a sacrificial layer on the extraction grid by angle evaporation comprises forming a sacrificial layer on the extraction grid by angle evaporation at an angle of seventy five degrees or more from a surface normal of the substrate.

61. The method of claim 59 wherein the act of forming emitters comprises:

forming emitter bodies by co-evaporating silicon monoxide and a metal; and

forming emitter tips by evaporating a material having a work function of less than four electron volts.